Charles Chen

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Research Interests

Signal processing, machine learning, robotics, computational neuroscience, control, and neuromorphic computing, with an emphasis biologically inspired systems.

Education

Columbia University, New York, NY — May 2026
Bachelor of Science in Computer Engineering — GPA: 3.7/4.00
Carnegie Mellon University, Pittsburgh, PA — May 2028
Masters of Science in ECE — GPA: 4.0/4.00

Research Experience

A2R Lab, Hanover, NH
Research Assistant — September 2024–Present

- Developed *TinyDroneRacer*, a fully autonomous racing stack for sub-50-g aerial robots operating under stringent onboard compute and sensing constraints.
- Designed a compact, multi-head convolutional neural network for onboard gate and clearance detection on a GAP8 AI-Deck.
- Improved existing TinyMPC-based controller with a novel heading-tracking model predictive controller formulation capable of going beyond pre-linearized points.
- Deployed onto a Brushless Crazyflie 2.1 and conducted experimental flights to evaluate gate traversal, heading-tracking error, obstacle-avoidance consistency, and course completion, achieving speeds of up to 2 m/s.

Publications & Preprints

[1] **Charles Chen**, Ishaan Mahajan, and Brian Plancher. "TinyDroneRacer: Fully Onboard Perception and Model Predictive Control for Drone Racing." *Manuscript in preparation*, 2026.

[2] Ishaan Mahajan, **Charles Chen**, Frederike Dümbgen, and Brian Plancher. "RAYA: Learning Where and When to Intervene for Recoverability-Aware Robot Control." *arXiv preprint 2609.21690, 2026.*

Industry Experience

SpaceX, Austin, TX
Embedded Firmware Intern — May 2025–August 2025

- Collaborated with enterprise and hardware teams to extract Ethernet port-speed data through MDIO registers across approximately 6 million power supplies, reducing system-level debugging by more than 600 hours per month.
- Ported ADC drivers from STM32H5 to STM32G0 microcontrollers, enabling current and voltage sensing for a next-generation power supply targeting a five-million-unit production run.
- Designed a DMA-based, high-throughput UART driver that increased debug-output speed by 90% and enabled sub-50-ms telemetry during firmware development.
- Prototyped analog-watchdog and PWM drivers to mitigate emergent hardware issues, avoiding approximately $800,000 in potential development costs.
- Reduced firmware binary size by 35 KB, enabling migration to a lower-cost MCU and an estimated $1.5 million reduction in production cost.

Shure Incorporated, Chicago, IL
Embedded Systems Intern — May 2024–August 2024

- Designed and deployed a Network Time Protocol application on embedded Linux and DHCP servers, synchronizing clocks to within 10 ms across approximately 1 million digital audio mixers.
- Implemented a network-socket client to independently validate synchronization with external NTP servers, achieving approximately 99% timing accuracy.
- Automated encryption of YAML configuration files across roughly 4 million products, saving an estimated 50 engineering hours per month.

Selected Projects

Medical Image Segmentation and Boundary Analysis for Cancer Imaging *MATLAB, Signal Processing*

- Analyzed medical images using classical and variational segmentation methods, including level sets, watershed segmentation, and region growing.
- Parameterized tumor boundaries and applied Fourier and moment-based descriptors to characterize boundary roughness and heterogeneity.
- Compared boundary descriptors with physician-drawn ground-truth segmentations to assess similarity and segmentation quality.

Finite Impulse Response Filter *Verilog, ModelSim, Questa, Synopsys, PrimeTime*

- Designed and functionally verified a FIR filter in Verilog using ModelSim and Questa.
- Performed synthesis and gate-level timing analysis with Synopsys tools and PrimeTime to validate timing closure.

FPGA Video Game *C, SystemVerilog*

- Designed a Geometry Dash–inspired 2D side-scrolling game on a Xilinx FPGA.
- Implemented a circular-buffer architecture for tile-map memory management and real-time rendering synchronized with on-chip C logic.

Technical Skills

Programming: C, C++, Python, MATLAB, Verilog, SystemVerilog, SystemC, MIPS, Java, JavaScript
Robotics & Machine Learning: Convolutional neural networks, embedded inference, computer vision, model predictive control, autonomous flight, dynamical-system simulation
Embedded & Hardware: Crazyflie 2.1, GAP8 AI-Deck, STM32, FPGA, UART/USART, SPI, I2C, CAN, LIN, USB, Ethernet, ADC, DAC, PWM, DMA, timers, watchdogs, RTC
Software & Tools: CMake, Bazel, GDB, JTAG, FreeRTOS, Linux, Bash, Vivado, ModelSim, Questa, Synopsys, PrimeTime
Networking: TCP/IP, DHCP, NTP, MDIO, Wireshark